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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/002,868	11/15/2001	Michael Belman	P05378US0	4795

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801 GRAND AVENUE
SUITE 3200
DES MOINES, IA 50309-2721

EXAMINER

SEFER, AHMED N

ART UNIT PAPER NUMBER

2826

DATE MAILED: 11/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

2826

Part of Paper No. 13

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 7/15/03 has been entered and claim 8 has been cancelled.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al. USPN 5,084,694 in view of Edwards, JR. et al. USPN 5,929,746.

Kikuchi et al disclose in fig. 1 a chip resistor comprising a substrate 1 having opposite parallel symmetrical top and bottom surfaces, and a central longitudinal plane of symmetry; separate and spaced first and second resistive layers 2 or thin film resistive layers (as in claim 3) on the top and bottom surfaces, respectively, electrically connected in parallel to each other and the top and the bottom surfaces of the substrate being symmetrically located with respect to and equidistant from the central longitudinal plane so that when electrical current

passes through the resistive layers, a temperature distribution within the substrate will be substantially symmetrical about the central longitudinal plane of the substrate for eliminating thermal bending thereof; wherein an area of the first resistive layer is substantially equal to that of the second resistive layer such that the chip resistor with both resistive layers tolerates higher instantaneous pulsed power than either layer could provide separately and individually; and first and second terminals 1C/3 for surface mounting, each terminal being electrically connected to the first and second resistive layers, the terminals being symmetrical about a central longitudinal plane, but do not specifically disclose a direct loading to a pick-and-place machine without concern for top-bottom orientation.

Edwards, JR. et al disclose (see col. 1, lines 9-21 and col. 5, lines 21-38) a direct loading to a pick-and-place machine.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate the teachings of Edwards, JR. et al with the device of Kikuchi et al since that would accommodate surface mounted resistors with a minimum adjustment of the machine as taught by Edwards, JR. et al.

As for claim 2, Edwards, JR. et al disclose (see col. 4, lines 1-5) thick film resistors.

4. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuchi et al in view of Edwards, JR. et al as applied to claim 1 above, and further in view of Thompson USPN 4,064,477.

The combined references disclose the device structure as recited in claim 1, but do not specifically teach the use of foil resistive layers.

Thompson discloses (see col. 1, lines 5-26) a foil resistive layer.

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Therefore, it would have been obvious to one skilled in the art at the time the invention was made to substitute the thin or thick film resistive layer of the prior art with a foil resistive layer, since that would allow a uniform current density.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (703) 605-1227.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601.

ANS

October 7, 2003


NATHAN J. FLYNN
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